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Investigation of the Instability of Low-Temperature Poly-Silicon Thin Film Transistors under a Negative Bias Temperature Stress

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In this work, we analyzed and correlated the hysteresis characteristics and instability under negative bias temperature instability (NBTI) stress in *p*-channel low-temperature poly-silicon (LTPS) thin-film transistors (TFTs). Positive V_{TH} shifts were observed under the NBTI stress. The hysteresis does not appear to be affected by the NBTI stress; however, when the V_G stress voltage is –40 V at 100°C, the hysteresis increases as the stress time increases and V_{TH} shifts with sub-threshold slope (*SS*) degradation. The hysteresis may increase under the extreme stress condition due to the generation of trap-states.

Keywords: LTPS, hysteresis, negative bias temperature (NBT) instability (NBTI), TFTs

1. INTRODUCTION

Low-temperature poly-crystalline silicon thin-film transistors (LTPS TFTs) have been widely investigated due to their high field-effect mobility and drive current for flat-panel applications such as the pixel elements of the active matrix organic light emitting diode (AMOLED).[1-3] The reliability issues of LTPS TFTs are very important in practical applications. In particular, because the LTPS TFTs must be designed using the CMOS inverter structure for driving circuit operation, the *p*-channel TFT will be subjected to negative bias temperature instability (NBTI), which maintains the "off" state of the pixel. In addition, the hysteresis phenomenon in LTPS TFTs resulting in a threshold voltage (V_{TH}) shift can cause image sticking in the display.[4] The residual image from the hysteresis, such that the previous display image remains in the subsequent image, may be a severe problem observed in conventional LTPS TFT pixels composed of 2-TFT.[5] Therefore, the hysteresis and NBTI are very important for the reliability of *p*-channel poly-Si TFTs. However, the correlation of the hysteresis and the NBTI degradation has not been well explored. Thus, in this paper, we investigate the hysteresis characteristics of the *p*-channel LTPS TFTs under NBTI stress.

2. EXPERIMENTAL PROCEDURE

Top-gate *p*-type LTPS TFTs were fabricated using the following process flow. First, 40-nm-thick *a*-Si layers were deposited on glass substrates via plasma-enhanced chemical vapor deposition (PECVD) and crystallized by excimer laser anneal (ELA). After patterning the films of polysilicon, 80/40-nm-thick TEOS/SiN_x gate insulator films were deposited. A 200-nm-thick Mo was later deposited as the gate metal by sputtering, while the source and drain (S/D) regions in the active region were implanted with boron and activated at 600°C by rapid thermal anneal (RTA). After forming the S/D, 50/400/50-nm-thick Ti/Al/Ti was deposited by sputtering to form the S/D contact. Silicon nitride was deposited by PECVD as a passivation layer. Finally, the samples were annealed in ambient air at 330°C for two hours. The TFT dimension used for this study was 7 × 20 μm^2 ($W \times L$). The

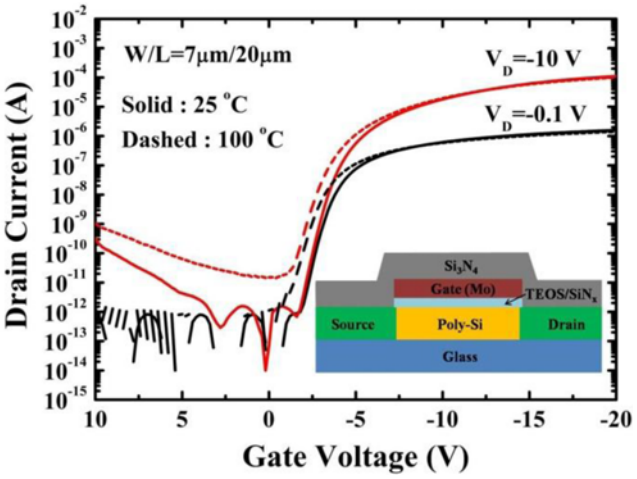

Fig. 1. The transfer characteristics of the LTPS TFTs at 25°C and 100°C. A schematic cross-section of the *p*-channel LTPS TFT is shown in the inset.

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constant current method was used for threshold voltage (V_{TH}) extraction, where the V_{TH} is defined as the bias of the gate voltage that forces the drain current to become (W/L) × 100 nA at V_D = 0.1 V.

Using an Agilent 4155B semiconductor parameter analyzer, electrical characteristic analysis of the LTPS TFTs was performed in ambient air and in the dark.

3. RESULTS AND DISCUSSION

The transfer characteristics of the LTPS TFT are presented in Fig. 1. The inset of Fig. 1 depicts a schematic cross-section of the device. The electrical parameters were extracted at 25°C. The V_{TH}, the sub-threshold slope (SS) and the on/off current ratio were –4.41 V, –0.46 V/decade and greater than 10^8, respectively. The field-effect mobility (m_{FE}) of 1.4 cm^2/V·s was extracted from the maximum trans-conductance (G_m).

The hysteresis characteristics of the LTPS TFT for linear region operation (V_D = –0.1 V) in the forward and reverse modes were investigated at 25°C and 100°C, respectively, as illustrated in Fig. 2. Forward and reverse gate voltage sweep were performed from 10 V to –20 V and vice versa. No significant hysteresis (also called ΔV_{hys}) effect was observed, regardless of V_D. However, the hysteresis effect at high temperature was smaller than that at room temperature. The charge de-trapping is faster as the temperature increases. In addition, the hysteresis increased as the sweep range of V_G increased, as illustrated in Fig. 3. The V_G sweep voltage was changed from 10 V to –5 V, –10 V, –15 V, and –20 V. This result can be explained because the energy-band bending is increased, resulting in an increase of the hole trapping as the negative V_G sweep voltage increases.

Figure 4 presents the transfer characteristics of the LTPS TFT before and after the NBTI stress (1000 s) with various

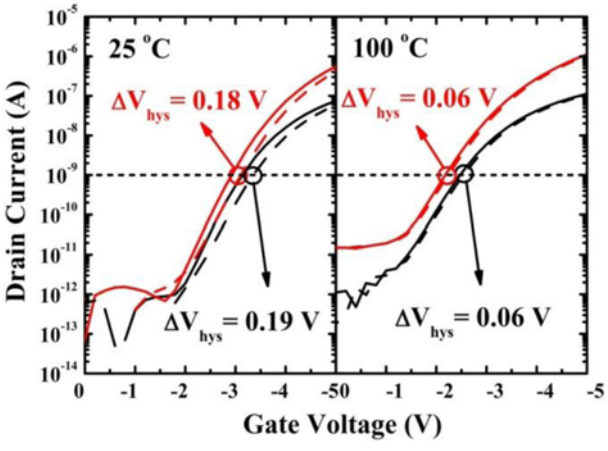

Fig. 2. The hysteresis characteristics of the LTPS TFT in the linear region of operation (V_D = –0.1 V) in the forward (solid line) and reverse modes (dashed line) at 25°C and 100°C.

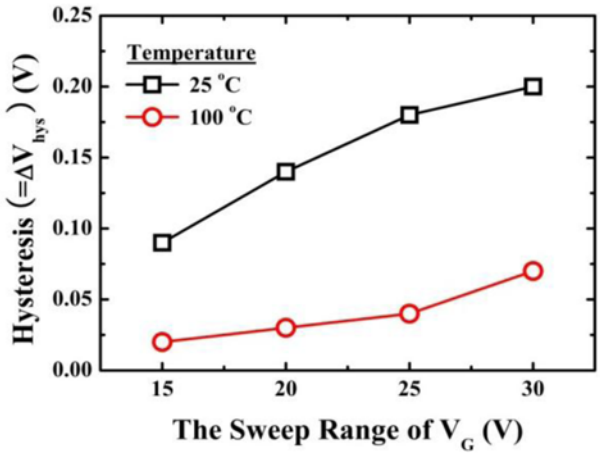

Fig. 3. A plot of the hysteresis vs. the sweep ranges of V_G in the LTPS TFT.

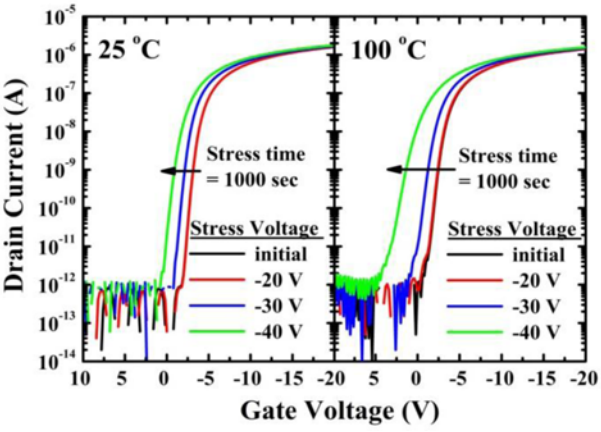

Fig. 4. The transfer characteristics of the *p*-channel LTPS TFT before and after NBTI stress time (1000 s) for various stress voltages for linear region operation (V_D = –0.1 V) at 25°C and 100°C.

stress voltages at V_D = –0.1 V. During the NBTI stress, the glass substrate was heated to the stress temperatures of 25°C and 100°C, and constant gate-stress voltages in the range of –20 V to –40 V were applied to the gate with the source/drain grounded. V_{TH} shifts to the positive direction even under the NBTI stress, and the degradation is significantly enhanced by a higher stress temperature and larger V_G stress. A negative V_{th} shift is typical for NBTI degradation.[6-8] Neglecting the opposite direction shift, the V_{TH} shift increases upon increasing the stress time and exhibits a power law dependence, as demonstrated in Fig. 5. Because the models of charge-trapping in gate dielectrics[9] cannot explain the linear fit of the log-log plot of ΔV_{TH} vs. the stress time, it is suggested that the NBTI stress is due to charge defect creation in the gate oxide and trap-state generation at the poly-Si/gate oxide interface and in the grain boundaries.[10] Considering the opposite direction of the NBTI shift, the generation of negative charge in the gate oxide under NBTI

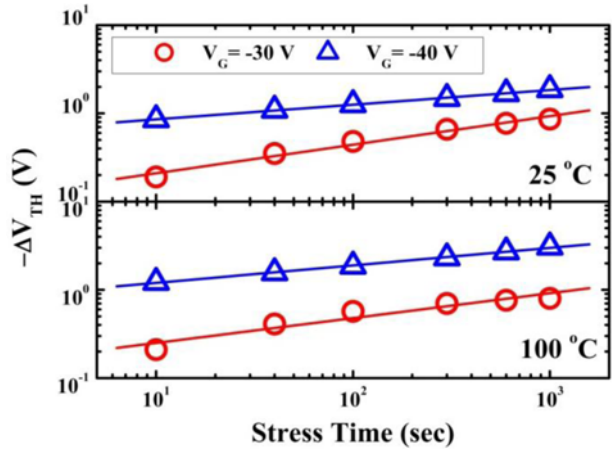

Fig. 5. The log-log plot of ΔV_{TH} vs. the NBTI stress time for various stress voltages in the LTPS TFT at 25°C and 100°C.

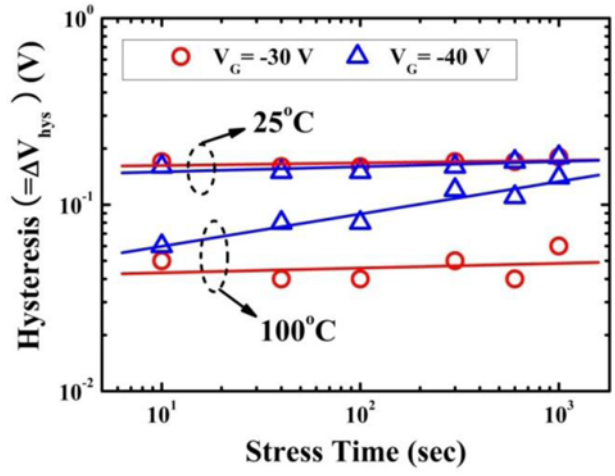

Fig. 6. Plot of the amount of the hysteresis vs. the NBTI stress time in the LTPS TFTs.

stress can be assumed in our experiments. The possible mechanism for this phenomenon is the negative-charge generation model.[11] The channel hot carriers leap over the surface potential barrier, break the ≡SiOH bonds and form an interface state ≡Si* and a fixed charge OH^-. Thus, fixed charges OH^- in the gate oxide or interface are generated under NBTI stress. As the electrical field across the gate insulator and silicon surface increases with increasing V_G, it could become sufficiently high to induce impact ionization, which is consistent with the increasing amount that V_{th} shifts as V_G increases (see Fig. 4).

Figure 6 shows the amount of hysteresis during the NBTI stress for various temperatures and V_G stress conditions. The hysteresis is almost identical before and after NBTI stress. The cause of the hysteresis is known to be caused by the charge trap/de-trap mechanism at the channel/gate oxide interface. Therefore, considering that the negative charge generation, not trap-states, is dominant under NBTI stress, as mentioned before, it is reasonable that the amount of hysteresis is not changed after NBTI stress.

For the V_G stress voltage of –40 V at 100°C, however, the hysteresis increases according to stress time. Under this stress condition, the V_{TH} shift with *SS* degradation was observed, while it was a parallel shift without *SS* degradation in the other stress condition, as demonstrated in Fig. 4. The *SS* of TFTs is known to be controlled by the interface trap states, while the small *SS* value implies low interface states.[12] Therefore, this result can be explained by the degradation of the device under extreme NBTI stress, exhibiting not only negative charge generation but also interface trap-state generation at the poly-Si/gate oxide interface. This mechanism explains why the hysteresis increases under the extreme stress condition. Even though the hysteresis is not affected by NBTI stress, where the negative charge appears to be generated at the poly-Si/gate oxide interface, it can be affected by the extreme stress condition due to the generation of trap-states therein.

4. CONCLUSIONS

In this paper, we investigated and correlated the hysteresis characteristics and NBTI stress in *p*-channel LTPS TFTs. We observed that the hysteresis is dependent on the applied V_G sweep ranges. As the V_{TH} shifts to the positive direction under NBTI stress, we demonstrate that negative charges were generated. In addition, the hysteresis is not affected by NBTI stress. However, in the extreme NBTI stress condition, the hysteresis increases according to stress time due to the generation of interface trap-states with negative-charge generation, which is consistent with the *SS* degradation from the transfer curve. This result indicates that the amount of the hysteresis is dependent on the number of charge traps/de-traps and is affected only by interface trap-state generation.

ACKNOWLEDGEMENTS

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